BEYOND SDRAM/FLASH/SRAM MEMORY CONTROLLER

Synchronous Dynamic and Asynchronous Static Memory Controller with shared IOs

OVERVIEW

Applications that must save on number of I/O rail voltages and/or pin count, but still require access to different types of memories can benefit from Beyond SDRAM/FLASH/SRAM controller. It allows you to connect various types and quantities of memory devices to your chip using only a single set of I/Os. SDRAM control part shares the I/Os with asynchronous control part to keep total pin count down. SDRAM and asynchronous control parts offer comprehensive device support and implement features for throughput optimization for application specific conditions. I/O control part handles I/O sharing between SDRAM and asynchronous parts. It also handles external arbitration interface which provides for memory sharing between multiple physical devices. The controller can also be used to access main boot device and offers boot option bus for various boot configuration options.

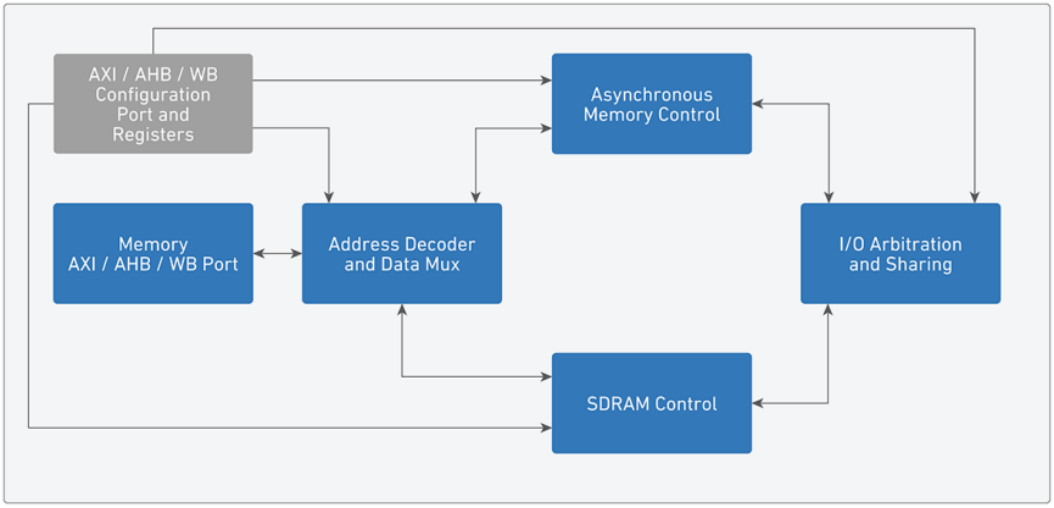
KEY BENEFITS

- Allows single I/O rail voltage for SDRAM and asynchronous devices
- Minimizes I/O count by sharing I/Os between SDRAM and asynchronous devices
- Single/double buffering for SDRAM data allows SDRAM memory throughput optimization
- Page access mode for asynchronous devices allows asynchronous memory throughput optimization

APPLICATIONS

- Mobile, automotive, telecom, control systems
- SoCs that require asynchronous and SDRAM external memory support, but are limited to single I/O rail voltage or have limited I/O resources available

BLOCK DIAGRAM



FEATURES

Internal Bus Interfaces

- AXI / AHB / WB compliant configuration interface used to:
  - Configure the controller
  - Initialize/suspend/wake external SDRAM devices using special register interface
- AXI / AHB / WB compliant memory access interface. Utilizes burst accesses to increase performance

SDRAM Control

- Programmable SDRAM device organization – provides comprehensive device support via register configuration
- Programmable memory width
- Programmable SDRAM features – burst length, auto pre-charge usage, cas latency etc.
- Programmable SDRAM timings
- Automatic SDRAM row management
- Automatic SDRAM refresh generation
- Compile time selectable single or double data buffering solution enables bandwidth optimization for application specific conditions

Asynchronous Memory Control

- Programmable asynchronous memory width and timing support wide variety of devices
- Asynchronous memory can be used as boot device
- Boot device variety achieved using power on configuration bus
- Throughput optimization using runtime configurable page mode accesses

I/O Muxing/Arbitration

- Arbitrates between internal SDRAM and Asynchronous device controllers
- Optionally includes external arbitration interface in its arbitration scheme – allows memory sharing between multiple devices

RELATED PRODUCTS

- Beyond DDR2/DDR SDRAM Memory Controller interleaves accesses from multi-port front-end when possible, maximizing utilization of memory control and data buses. This utilizes higher memory bandwidth capabilities as additional latency cycles can be used for housekeeping operations – bank, row and refresh management

BEYOND SEMICONDUCTOR

Beyond Semiconductor is addressing challenges of systemic complexity in today's electronic devices, empowering its customers to create new experiences for end users.
Initially known for its processor expertise, Beyond quickly gained acceptance among top semiconductor companies and evolved into global company leveraging processing, software and system-wide view competence to provide its customers with effectively designed IP and ASICs.

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