BEYOND MAC 10/100/1000 ETHERNET CONTROLLER

IEEE 802.3 & IEEE 802.3 – 2002 Compliant IP Core

OVERVIEW

The Beyond MAC (Media Access Controller) 10/100/1000 Ethernet Controller consists of a synthesizable Verilog RTL core that provides all features necessary to implement the Layer 2 protocol of the Ethernet standard. It is designed to run according to the IEEE 802.3 and IEEE 802.3-2002 specifications that define the 10 Mbps, 100 Mbps and 1000Mbps Ethernet standards, respectively. An external PHY is needed for the complete Ethernet solution.

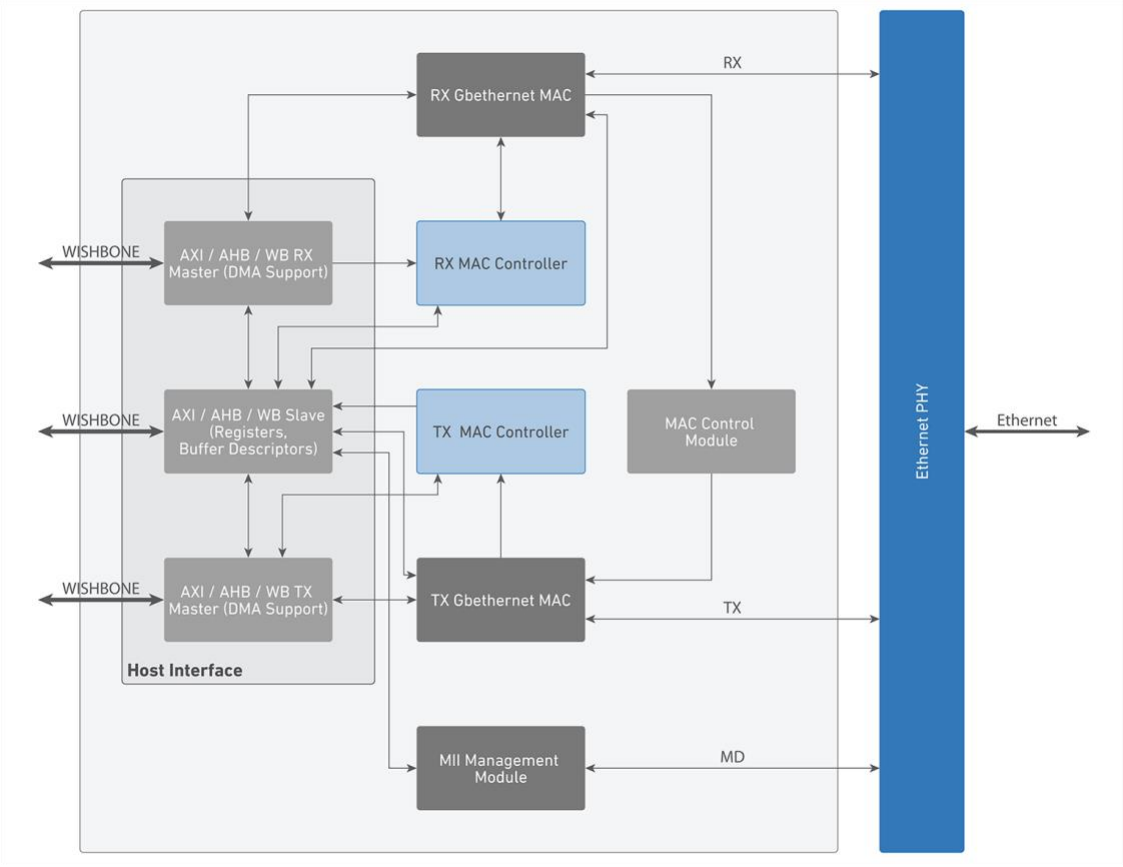
KEY BENEFITS

- IEEE 802.3-2000 compatible 10/100/1000 Mbps operation modes
- Configurable number of transmit and receive buffer descriptors (up to 128 total)
- AXI, AHB or WISHBONE interconnect option

APPLICATIONS

- Internet, networking and telecom

BLOCK DIAGRAM



FEATURES

Data Link Layer

- IEEE 802.3-2002 specification with preamble, start-of-frame delimiter (SFD), frame padding generation and cyclic redundancy code (CRC) generation and checking is fully implemented
- Supports 10/100 Mbps or 1000 Mbps operation (selectable via a core configuration registers)
- Supports full- and half-duplex operation (selectable via a core configuration registers)
- CSMA/CD protocol for half-duplex operation
- Supports frame-extension in 1000 Mbps half-duplex mode
- IEEE 802.3x flow-control for full duplex operation
- Variety of flexible address filtering modes
- Detection of too long or too short packets (configurable length limits)
- Complete status for TX/RX packets

PHY Interfaces

- IEEE 802.3-2002 Media Independent
- Interface (MII) and Gigabit Media
- Independent Interface (GMII)
- MDIO Master interface for PHY device configuration and management

Transmit (TX) / Receive (RX) Dual Port Synchronization Rams

- Configurable TX threshold level
- RX transfer started as soon as data synchronized
- Configurable RAMs sizes – up to 16kB

DMA Controller

- Internal RAM for holding up to 128 TX/RX buffer descriptors
- Configurable number of TX/RX buffer descriptors
- Supports transmission and reception of packets that are bigger than standard packets (up to 16-Kbyte) – jumbo frames
- Interrupt generation on all events
- Big/little endian data byte ordering

Host Interface

- Two interrupts lines with corresponding interrupt mask register (split TX and RX operation)
- Clock switch control port (10/100 or 1000 Mbit)
- Optional status counters

Supported SoC Bus Interfaces

The core is available with support for any of the following interconnect options:

- AMBA AXI / AHB / APB as appropriate
- AMBA AXI
- WISHBONE Master and Slave interfaces (efficient burst transfers supported for Master)
- Other buses: for additional options please contact sales@beyondsemi.com

RELATED PRODUCTS

- Beyond IPsec Core provides implementation of an Encapsulating Security Payload (ESP) protocol, a key member of the IPsec protocol suite, which is widely used for securing network traffic between the two endpoints that communicate over the Internet.
- The Beyond VPN Subsystem is a bundle of semiconductor IP cores and software modules, which provide key functionality of modern VPN systems based on the IPsec protocol suite. The components of the bundle are designed for easy integration with widely deployed open-source solutions and thus enable rapid development of security gateways.

BEYOND SEMICONDUCTOR

Beyond Semiconductor is addressing challenges of systemic complexity in today's electronic devices, empowering its customers to create new experiences for end users.
Initially known for its processor expertise, Beyond quickly gained acceptance among top semiconductor companies and evolved into global company leveraging processing, software and system-wide view competence to provide its customers with effectively designed IP and ASICs.

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