

Beyond TAP Controller

Introduction

The Beyond TAP Controller is a fully IEEE 1149.1-2001 compatible JTAG Test Access Port (TAP) Controller. It is used for development / debugging purposes (Boundary Scan, Memory BIST and Debugging) and is as such an interface between the Boundary Scan / Memory BIST / Beyond Debug Interface Controller (which connects to the Beyond processor(s) and Beyond peripheral interface cores) and external debugger / emulator testing device (commercial or Beyonds).

For information on various licensing options or other IP cores please contact sales@beyondsemi.com or visit our website at <http://www.beyondsemi.com>. Some features may be omitted in this datasheet or might be shortly available. If you require something not listed here or if in doubt we encourage you that you contact our sales department at sales@beyondsemi.com.

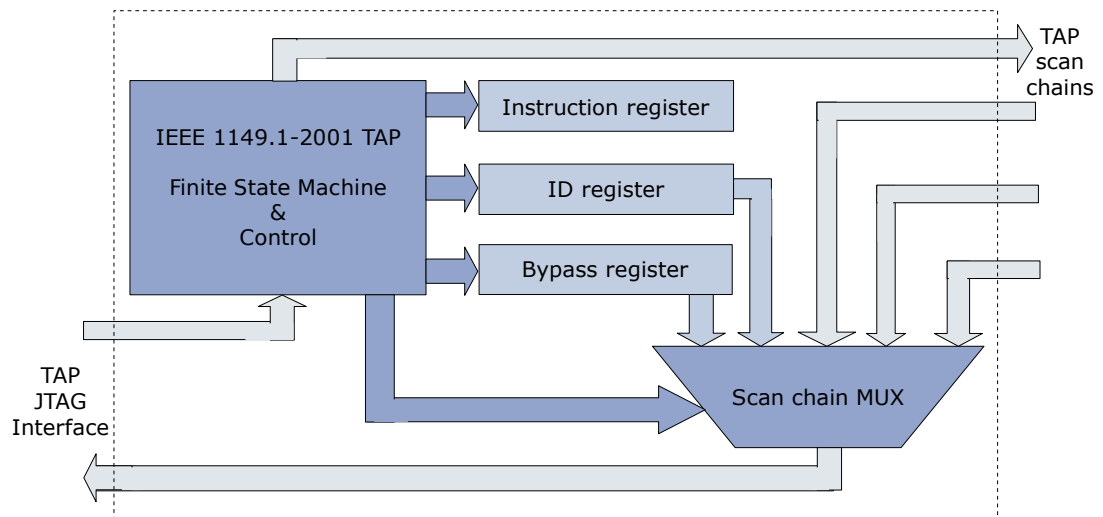
Features

- IEEE 1149.1-2001 compatible JTAG interface (TRST, TCK, TMS, TDI and TDO) to the external debugger / emulator testing device
- Supported instructions:
 - All mandatory public instructions (BYPASS, SAMPLE/PRELOAD and EXTEST)
 - Optional public instruction (IDCODE)
 - Private instructions (DEBUG and MBIST)
- Supported scan chain registers:
 - Internal Bypass register
 - Internal ID register
 - External Boundary Scan register
 - External Debug Interface register
 - External Memory BIST register

Architecture

Figure below shows the general architecture of the Beyond TAP Controller IP core. It consists of following building blocks:

- IEEE 1149.1-2001 compatible TAP Finite State Machine
- Instruction register
- Internal scan chain ID register
- Internal scan chain Bypass register
- Multiplexer for scan chain registers



Beyond TAP IP Core

Easy and Quick Start

Deliverables

- Full Verilog RTL source
- Extensive Test Bench
- Documentation
- Linux Driver
- Free Engineering support

Target Applications

- Boundary Scan testing
- Internal memory testing with Memory BIST
- Software uploading and debugging with Beyond Debug Interface Controller
- Beyond peripheral interface cores initialization with Beyond Debug Interface Controller

Data Sheet

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