

Beyond VGA Display Controller

Introduction

The Beyond VGA Display Controller IP Core provides VGA capabilities for embedded systems. It supports both CRT and LCD displays with user programmable resolutions and video timings, thus providing compatibility with almost all available LCD and CRT displays.

The core supports a number of color modes, including 32bpp, 24bpp, 16bpp, 8bpp gray-scale, and 8bpp-pseudo color. The video memory is located outside the primary core, thus providing the most flexible memory solution possible. It can be located on-chip or off-chip, shared with the system's main memory (VGA on demand) or be dedicated to the VGA system. Image data is fetched automatically via the AHB or WISHBONE Master interface, making this an ideal "program-and-forget" video solution. More demanding video applications, like streaming video or video games, can benefit from the video-bank-switching function. Flicker and cluttered images are reduced by switching between video-memory pages on vertical retrace.

The horizontal, vertical, and composite synchronization polarization levels, as well as the blanking polarization level are programmable by software.

For information on various licensing options or other IP cores please contact sales@beyondsemi.com or visit our website at <http://www.beyondsemi.com>. Some features may be omitted in this datasheet or might be shortly available. If you require something not listed here or if in doubt we encourage you that you contact our sales department at sales@beyondsemi.com.

Features

- Horizontal and vertical image scaling by integer factors
- CRT and LCD display support
- Separate VSYNC/HSYNC and composite (CSYNC) synchronization signals
- Composite BLANK signal
- User programmable video timing
- User programmable video resolutions
- User programmable video control signals polarity.
- 32bpp, 24bpp and 16bpp color modes
- 8bpp gray-scale and 8bpp pseudo-color modes
- Supports video bank switching during vertical retrace
- AHB or WISHBONE Rev.B3 compliant Slave (32 bit) and Master (32/64 bit) interfaces
- Operation from a wide range of independent System/Pixel input clock frequencies
- Static synchronous design
- Full synthesizability

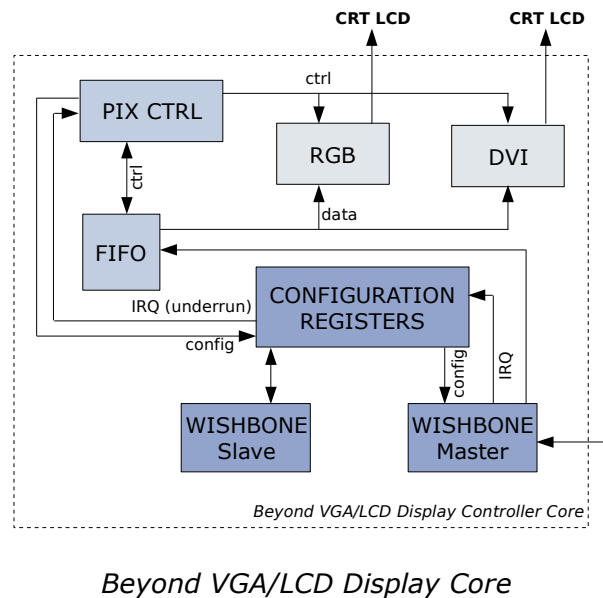
Easy and Quick Start

Deliverables

- Full Verilog RTL source
- Extensive Test Bench
- Documentation
- Linux Driver
- Free Engineering support

Target Applications

- Embedded GUI
- Embedded multimedia



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