

# Beyond UART 16550 Serial Controller

## Introduction

Beyond UART (Universal Asynchronous Receiver/Transmitter) 16550 Serial Controller IP core translates data between parallel and serial interfaces, and adds/removes start, stop bits, and optionally parity bit. It can be used to communicate with other external devices using a serial cable and RS232 protocol. This core is compatible with industry standard National Semiconductors 16550D device except for scratch register which is not implemented. Additionally CPU can read values of divisor latch and fill levels of transmitter and receiver FIFOs. On power-up/reset Beyond UART starts in 16450 mode.

For information on various licensing options or other IP cores please contact [sales@beyondsemi.com](mailto:sales@beyondsemi.com) or visit our website at <http://www.beyondsemi.com>. Some features may be omitted in this datasheet or might be shortly available. If you require something not listed here or if in doubt we encourage you that you contact our sales department at [sales@beyondsemi.com](mailto:sales@beyondsemi.com).

## Features

### Features

- compatible with PC16550D / 16450
- FIFO depth of 16 bytes in 16550 mode
- MODEM control functions
- programmable serial interface:
  - number of data bits (5 – 8)
  - number of stop bits
    - 1 and 1,5 for (5 data bits)
    - 1 and 2 (6, 7, 8 data bits)
  - false start bit detection
  - internal diagnostic (loopback, error simulation)
  - line break generation and detection
  - prioritized interrupts
  - readable Divisor latch value
  - readable transmitter and receiver FIFO fill levels

### Supported SoC Bus Interfaces

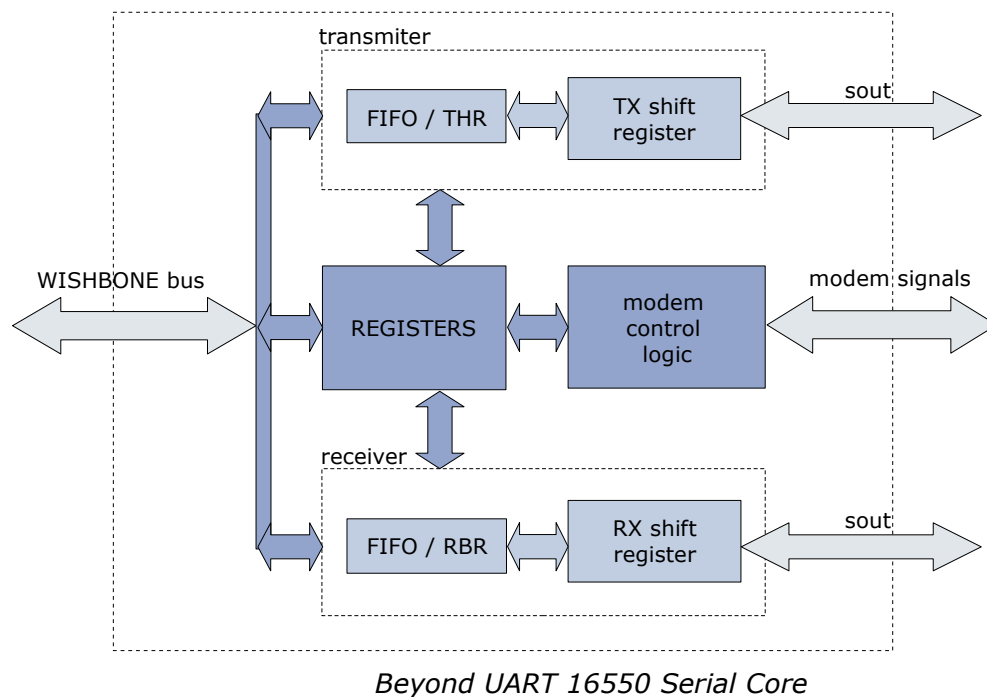
The core is available with support for any of the following interconnect options:

- AMBA
  - APB Slave Interface
- WISHBONE Slave Rev. B.3 compliant interfaces
- Other buses: for additional options please contact [sales@beyondsemi.com](mailto:sales@beyondsemi.com)

## Architecture

Figure below shows the general architecture of the Beyond UART 16550 Serial Controller IP core. It consists of following building blocks:

- Bus interface
- Modem control logic
- Internal registers
- Transmitter logic
  - FIFO / THR register
  - TX shift register
- Receiver logic
  - FIFO / RBR register
  - RX shift register



## Easy and Quick Start

### Deliverables

- Full Verilog RTL source
- Extensive Test Bench
- Documentation
- Linux Driver
- Free Engineering support

### Target Applications

- Networking
- Embedded
- Portable and wireless
- Home entertainment consumer electronics

# Data Sheet

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