

Beyond SDRAM/FLASH/SRAM Memory Controller

Introduction

Almost every SoC produced today uses some kind of external memory, because large embedded memories can be costly in terms of price, overall die size and power consumption. Beyond SDRAM/FLASH/SRAM Memory Controller IP Core provides access to external asynchronous static and synchronous dynamic memory devices for SoC designs using multiport AHB or WISHBONE SoC interconnect bus as internal bus. A wide variety of different memory device organizations and speeds are supported. Beyond SDRAM/FLASH/SRAM Memory Controller IP Core also uses a lot of optional, pre-synthesis parameters, which makes it configurable for use in a wide variety of applications.

For information on various licensing options or other IP cores please contact sales@beyondsemi.com or visit our website at <http://www.beyondsemi.com>. Some features may be omitted in this datasheet or might be shortly available. If you require something not listed here or if in doubt we encourage you that you contact our sales department at sales@beyondsemi.com.

Features

Beyond SDRAM/FLASH/SRAM Memory Controller IP Core consists of several modular units.

Memory Interface

- External control signals for standard SDRAM memory devices
- External control signals for standard asynchronous static devices
- Software configurable external memory device data width for each chip select
- Supported widths are 8, 16, 32 and 64 bits for SDRAM devices and 8, 16 and 32 for asynchronous devices
- Register interface for software initiated SDRAM initialization sequence
- Support for asynchronous page mode static devices
- Possible SDRAM burst sizes are 1, 2, 4 and 8
- Software programmable asynchronous static memory device timing parameters for every chip select
- Software programmable SDRAM memory device timings
- Software programmable SDRAM memory organization
- Open row track keeping logic for SDRAM devices. Allows lower access latency
- Software programmable SDRAM address generation mode. Two modes are supported: Bank/Row/Column and Row/Bank/Column
- Automatic SDRAM refresh generation
- Register interface for software initiated suspend operation to external memory devices
- The data organization can be selected before synthesis and can be either big or little endian

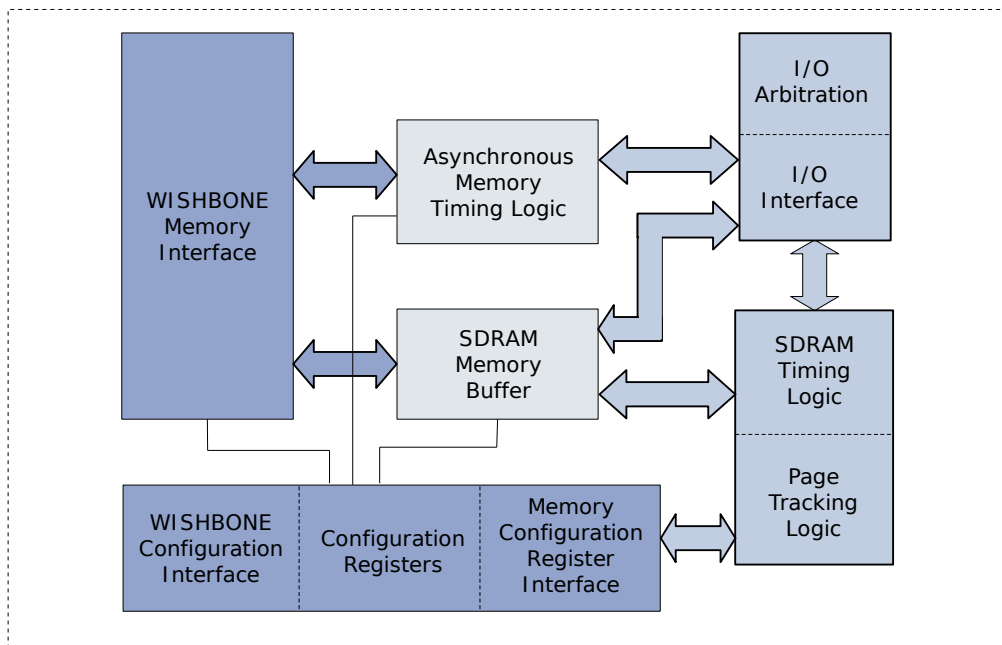
Supported SoC Bus Interconnect

The core is available with support for any of the following interconnect options:

- AMBA:
 - AHB for memory access ports
 - AHB or optionally APB for configuration port (for setting memory timings, etc.)
- WISHBONE Rev. B.3 compliant interfaces (efficient burst transfers supported)
 - All WISHBONE burst, classic and single transfer cycles are supported for write and read operations

Core Internals

- Most of the software programmable core configuration and timing parameters can be hardwired using the core's define file. This enables its usage in highly specific, area critical applications, for which the configuration and speed of external devices is known in advance. Registers can be implemented for general purpose applications, for which the speed and configuration of external memories is not known in advance.
- Read Buffer size for synchronous memory devices is configurable before synthesis and can be 2, 4, 8, 16 or 32 32-bit locations. Larger buffer size in combination with other configuration parameters will increase the core's performance as well as its size.



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Easy and Quick Start

Deliverables

- Full Verilog RTL source
- Example constraints
- Extensive verification suite including test bench and simulation scripts
- Example synthesis scripts
- Documentation
- Free Engineering support

Target Applications

- Internet, networking and telecom
- Embedded
- Portable and wireless
- Home entertainment consumer electronics
- Automotive

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