

# Beyond PCI 32 Bridge Controller

## Introduction

Today, the PCI bus is the number-one device connectivity standard on the market to integrate modern embedded applications into bigger systems. Beyond PCI 32 Bridge IP Core is built according to PCI specification Rev. 2.2 (or lower) and provides a backend connection that is multiport AHB or WISHBONE open-standard compatible. Since standardized backend is rarely seen in common IP cores, the architecture-independent interface, which can be used in a wide variety of applications, is the PCI Bridge IP Core's major benefit.

For information on various licensing options or other IP cores please contact [sales@beyondsemi.com](mailto:sales@beyondsemi.com) or visit our website at <http://www.beyondsemi.com>. Some features may be omitted in this datasheet or might be shortly available. If you require something not listed here or if in doubt we encourage you that you contact our sales department at [sales@beyondsemi.com](mailto:sales@beyondsemi.com).

## Features

The Beyond PCI 32 Bridge Controller consists of several modular units.

### PCI Interface

- PCI 2.2 compliant 32bit, 66MHz Initiator and Target interface
- Zero wait state burst operation
- Parameterized number of synthesizable, fully programmable images (default one, maximum 6 images) with address translation capability and 4KB to 1GB image size for access from PCI bus to address space on WISHBONE bus
- Programmable image address space mapping (I/O or memory space)
- PCI transaction ordering requirements; use of posted writes and delayed reads in either direction
- Single delayed transaction support in either direction
- Supported initiator functions:
  - Memory Read, Memory Read Line, Memory Read Multiple, Memory Write commands
- IO Read and Write commands
- Configuration Read and Write commands:
  - Interrupt Acknowledge command
  - Support of linear burst ordering
- Supported Target functions:
  - Memory Read, Memory Read Line, Memory Read Multiple, Memory Write, Memory Write and Invalidate commands
  - IO Read and Write commands
  - Configuration Read and Write commands
  - Support of linear burst ordering
  - Software configurable support for memory access optimizing commands
- Fully transparent WISHBONE interface operation, controllable on image by image basis with proper software settings of configuration registers

## **WISHBONE Interface**

- WISHBONE clock independent of PCI clock
- WISHBONE SoC bus revision B.1 compliant with separate Master and Slave interfaces
- Zero wait state burst operation
- Parameterized number of synthesizable, fully programmable images (default one, maximum 5 images) with address translation capability and 4KB to 1GB image size provided for access from WISHBONE bus to address space on PCI bus
- Fully transparent PCI bus command

usage, controllable on image by image basis with proper settings of configuration registers

## **Core Internals**

- Provision of two possible parameterized implementations – HOST (used for host bridging with WISHBONE SoC bus as host bus) and GUEST (used for expansion bus bridging with WISHBONE SoC bus as expansion bus)
- Four synthesizable, dual port FIFOs with parameterized depth
- Extended configuration space, implemented for additional software programmable features of the core

## **General Description**

Beyond PCI Bridge IP Core is PCI specification Rev. 2.2 compliant but can also be used in systems designed according to lower versions, since the PCI is backwards compatible. A set of pre-synthesis parameters is defined in a separate file and offers a wide variety of implementations – from high performance to low cost (in terms of resource utilization). The Core is targeting FPGA as well as ASIC SoC implementations.

## Easy and Quick Start

### Deliverables

- Full Verilog RTL source
- Extensive Test Bench
- Documentation
- Linux Driver
- Free Engineering support

### Target Applications

- Internet, networking and telecom
- Embedded
- Home entertainment consumer electronics

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