

Beyond MAC 10/100/1000 Ethernet Controller

Introduction

The Beyond MAC (Media Access Controller) 10/100/1000 Ethernet Controller consists of a synthesizable Verilog RTL core that provides all features necessary to implement the Layer 2 protocol of the Ethernet standard. It is designed to run according to the IEEE 802.3 and IEEE 802.3-2002 specifications that define the 10 Mbps, 100 Mbps and 1000Mbps Ethernet standards, respectively. An external PHY is needed for the complete Ethernet solution.

For information on various licensing options or other IP cores please contact sales@beyondsemi.com or visit our website at <http://www.beyondsemi.com>. Some features may be omitted in this datasheet or might be shortly available. If you require something not listed here or if in doubt we encourage you that you contact our sales department at sales@beyondsemi.com.

Features

Ethernet Features

- IEEE 802.3-2002 specification with preamble, start-of-frame delimiter (SFD), frame padding generation and cyclic redundancy code (CRC) generation and checking is fully implemented
- Supports 10/100 Mbps or 1000Mbps operation (selectable via a core configuration registers)
- Supports full- and half-duplex operation (selectable via a core configuration registers)
- CSMA/CD protocol for half-duplex operation
- Supports frame-extension in 1000 Mbps half-duplex mode
- IEEE 802.3x flow-control for full-duplex operation
- Variety of flexible address filtering modes
- Detection of too long or too short packets (configurable length limits)
- Supports transmission and reception of packets that are bigger than

- standard packets (up to 16-Kbyte)
- Complete status for TX/RX packets
- IEEE 802.3-2002 Media Independent Interface (MII) and Gigabit Media Independent Interface (GMII)
- MDIO Master interface for PHY device configuration and management
- Internal RAM for holding 128 TX/RX buffer descriptors
- Interrupt generation on all events

Supported SoC Bus Interfaces

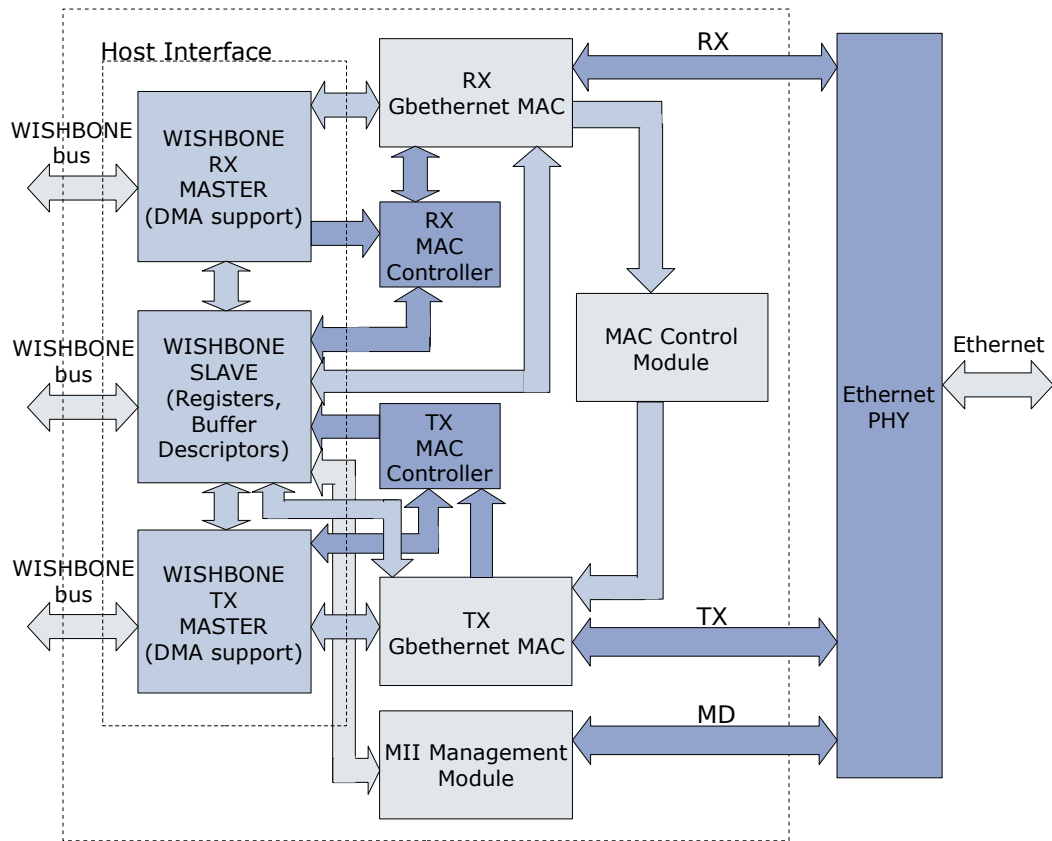
The core is available with support for any of the following interconnect options:

- AMBA:
 - AHB for Master Interface
 - AHB for optionally APB for Slave interface (used for core control)
- WISHBONE Master and Slave Rev. B.3 compliant interfaces (efficient burst transfers supported for Master)
- Other buses: for additional options please contact sales@beyondsemi.com

Architecture

Figure below shows the general architecture of the Beyond MAC 10/100/1000 IP core. Beyond MAC 10/100/1000 IP core consists of several building blocks:

- The MAC Control module which together with Rx Gbethernet MAC and Tx Gbethernet MAC performs full duplex control function
 - The Rx Gbethernet MAC performs receive function
- The Tx Gbethernet MAC performs transmit function
- The host interface which consist of:
 - The Wishbone Rx Master module
 - The Wishbone Tx Master module
 - The Wishbone Slave module which includes registers and buffer descriptors
 - The MII Management module



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Easy and Quick Start

Deliverables

- Full Verilog RTL source
- Extensive Test Bench
- Documentation
- Linux Driver
- Free Engineering support

Target Applications

- Internet, networking and telecom applications

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