

Beyond GPIO Controller

Introduction

Beyond GPIO Controller IP core is user-programmable general-purpose I/O controller. Its use is to implement functions that are not implemented with the dedicated controllers in a system and require simple input and/or output software controlled signals.

For information on various licensing options or other IP cores please contact sales@beyondsemi.com or visit our website at <http://www.beyondsemi.com>. Some features may be omitted in this datasheet or might be shortly available. If you require something not listed here or if in doubt we encourage you that you contact our sales department at sales@beyondsemi.com.

Features

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- Number of general-purpose I/O signals is user selectable and can be in range from 1 to 32. For more I/Os several GPIO cores can be used in parallel
- All general-purpose I/O signals can be bi-directional (external bi-directional I/O cells are required in this case)
- All general-purpose I/O signals can be three-stated or open-drain enabled (external three-state or open-drain I/O cells are required in this case)
- General-Purpose I/O signals programmed as inputs can cause an interrupt request to the CPU
- General-purpose I/O signals programmed as inputs can be registered at raising edge of system clock or at user programmed edge of external clock
- All general-purpose I/O signals are programmed as inputs at hardware reset

- Auxiliary inputs to GPIO core to bypass outputs from RGPIO_OUT register
- Alternative input reference clock signal from external interface
- Extremely configurable (implementation of registers, external clock inverted versus negedge flip-flops etc.)

Supported SoC Bus Interfaces

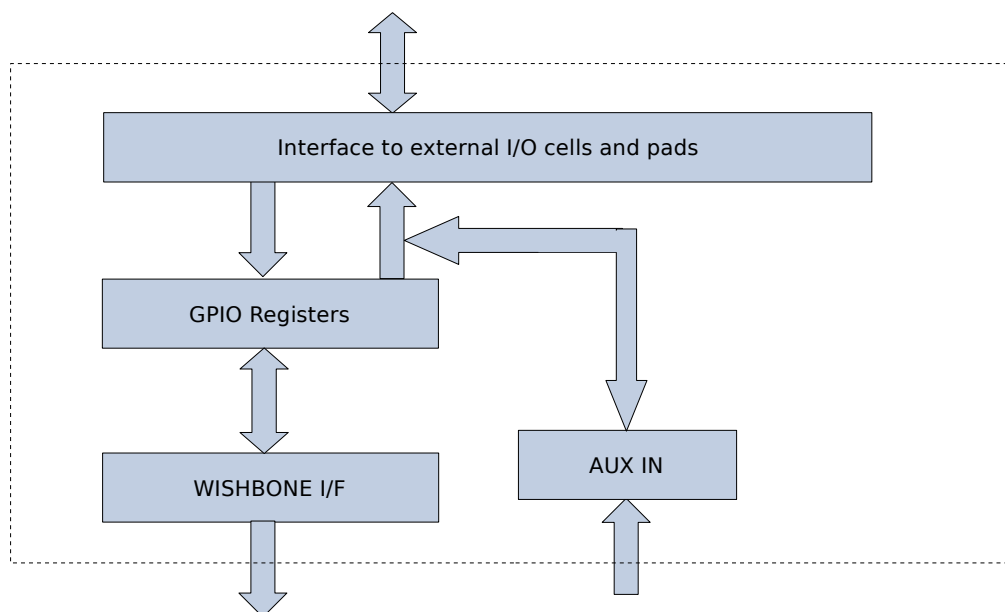
The core is available with support for any of the following interconnect options:

- AMBA
 - AHB or optionally APB
- WISHBONE Slave Rev. B.3 compliant interfaces
- Other buses: for additional options please contact sales@beyondsemi.com

Architecture

Figure below shows the general architecture of the Beyond GPIO IP core. It consists of following building blocks:

- SoC Bus interface
- GPIO registers
- Auxiliary inputs
- Interface to external I/O cells and pads



Beyond GPIO Controller building blocks

Easy and Quick Start

Deliverables

- Full Verilog RTL source
- Extensive Test Bench
- Documentation
- Linux Driver
- Free Engineering support

Target Applications

- Embedded
- Portable and wireless
- Home entertainment consumer electronics

Data Sheet

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