

Beyond AC97 Audio Controller

Introduction

Beyond AC97 Audio Controller IP Core is designed to enable easy control of external AC97 CODECs using multi port AMBA AHB/APB or WISHBONE SOC interconnect. It is implemented in a way to minimize audio data handling by SOC processor via built-in dedicated audio DMA engine. External interface supports one external AC97 revision 2.3 compliant audio CODEC with 6 output (3 of them can be Double Rate Audio) and 3 input channels.

For information on various licensing options or other IP cores please contact sales@beyondsemi.com or visit our website at <http://www.beyondsemi.com>. Some features may be omitted in this datasheet or might be shortly available. If you require something not listed here or if in doubt we encourage you that you contact our sales department at sales@beyondsemi.com.

Features

Beyond AC97 Audio Controller main features are:

Audio Features

- Fixed 48kHz audio support
- Hardware variable sample rate support from 8kHz to 48kHz (up to 96kHz with Double Rate Audio enabled)
- Double Rate Audio support for Left, Right and Center channels
- 16, 18 and 20-bit sample size support
- Mono, stereo or multichannel (1, 2, 4 or 6 channels) audio output support
- Stereo Input and dedicated Mono microphone Input Channel support (all together 3 input channels)
- Power management support (individual subsections or full power-down mode)
- Full access to CODEC registers (tone, loudness, 3D stereo enhancement, etc.)

Supported SoC Bus Interfaces

The core is available with support for any of the following interconnect options:

- AMBA
 - AHB for Master Interface
 - AHB for optionally APB for Slave Interface
- WISHBONE Master and Slave Rev. B.3 compliant interfaces (efficient burst transfers supported for Master)
- Other buses: for additional options please contact sales@beyondsemi.com

Interface Features

- Can operate as Slave only audio controller (Master doesn't need to be connected)
- Integrated audio DMA engine using Master Interface
- Full audio stream/channel decoding (through DMA)
- All channels can be configured to use any stream and/or sub-stream data (including stereo channels)

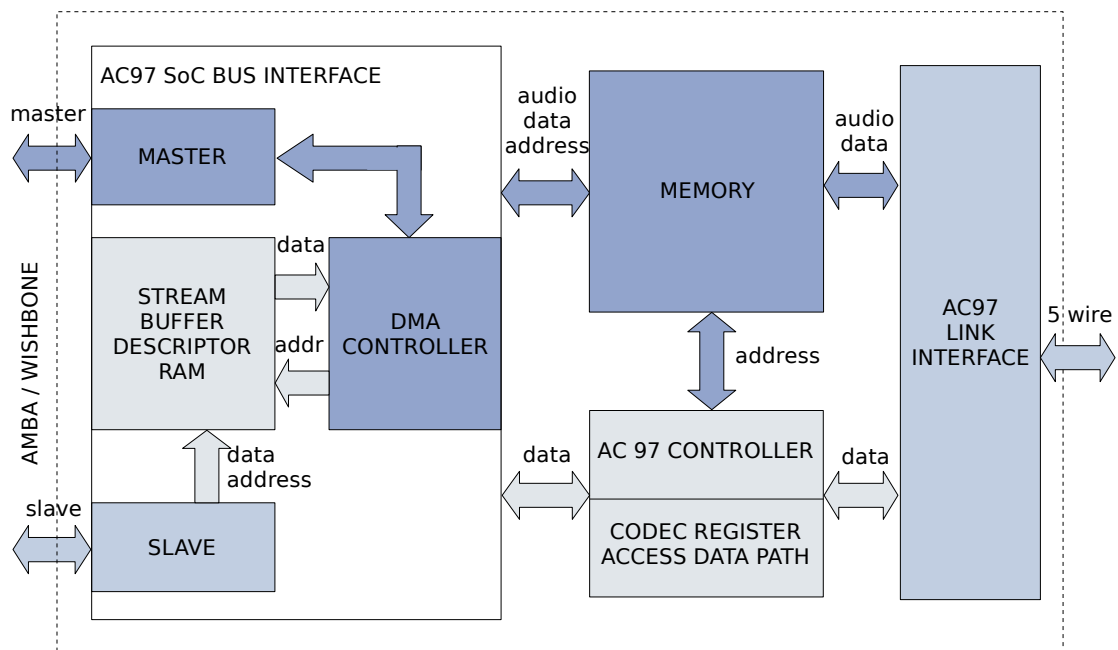
Memory Features

- System memory double-buffering supported
- Internal memory double-buffering supported
- Fully configurable internal memory support
- Configurable stream descriptor memory size

Architecture

Figure below shows the general architecture of the Beyond AC97 Audio IP core. It consists of following building blocks:

- AC97 link interface
- Internal memory
- AC97 controller with CODEC register access
- AC97 SoC bus interface:
 - Slave interface (AMBA/WISHBONE)
 - Stream buffer descriptor RAM
 - DMA controller
 - Master interface (AMBA/WISHBONE)



Beyond AC97 Audio Controller IP Core

Easy and Quick Start

Deliverables

- Full Verilog RTL source
- Extensive Test Bench
- Documentation
- Linux Driver
- Free Engineering support

Target Applications

- Embedded
- Portable and wireless
- Home entertainment consumer electronics

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