

Beyond Kiwi Platform

Introduction

Beyond Kiwi Platform, SOC/ASIC design, is SILICON PROVEN 32-bit microcontroller design that allows customers to take it as a base design and modify it into their own SOC/ASIC. Beyond Kiwi SOC/ASIC is delivered as synthesizable Verilog RTL with Verilog test benches, simulation and synthesis scripts, software development tools for the processor and documentation.

Features

Beyond Kiwi Platform consists of several modular units.

Beyond BA12 32-Bit RISC/DSP

- 32-bit RISC/DSP soft core delivering 133 MIPS performance @ 133MHz worst-case conditions
- Complete software development toolchain
- Optional L1 caches 4-8KB caches
- Optional MMUs (virtual memory, page protection)
- Power management unit
- Advanced debug unit allowing in-circuit debugging, hardware breakpoints, complex breakpoint and watchpoint conditions
- Integrated tick timer
- Programmable interrupt controller
- Optional custom instructions

Beyond UART 16550 Serial Controller

- Compatible with "standard" 16550D
- FIFOs can be removed

Beyond Debug Interface

- Access to internal CPU registers, WISHBONE and QMEM buses over TAP interface

Beyond TAP Controller

- fully compliant with IEEE 1149.1-2001 standard

Embedded memory

- RAM
- ROM

Easy and Quick Start

Deliverables

- Synthesizable RTL description in Verilog HDL
- Test bench in Verilog HDL
- Software development tools for Cygwin on Windows and Linux
- Engineering support

Software Development Tools

- Integrated Development Environment
- ANSI C and Java compilers
- Debugger, linker, assembler and utilities
- Architectural simulator
- Supported platforms Cygwin on Windows and Linux

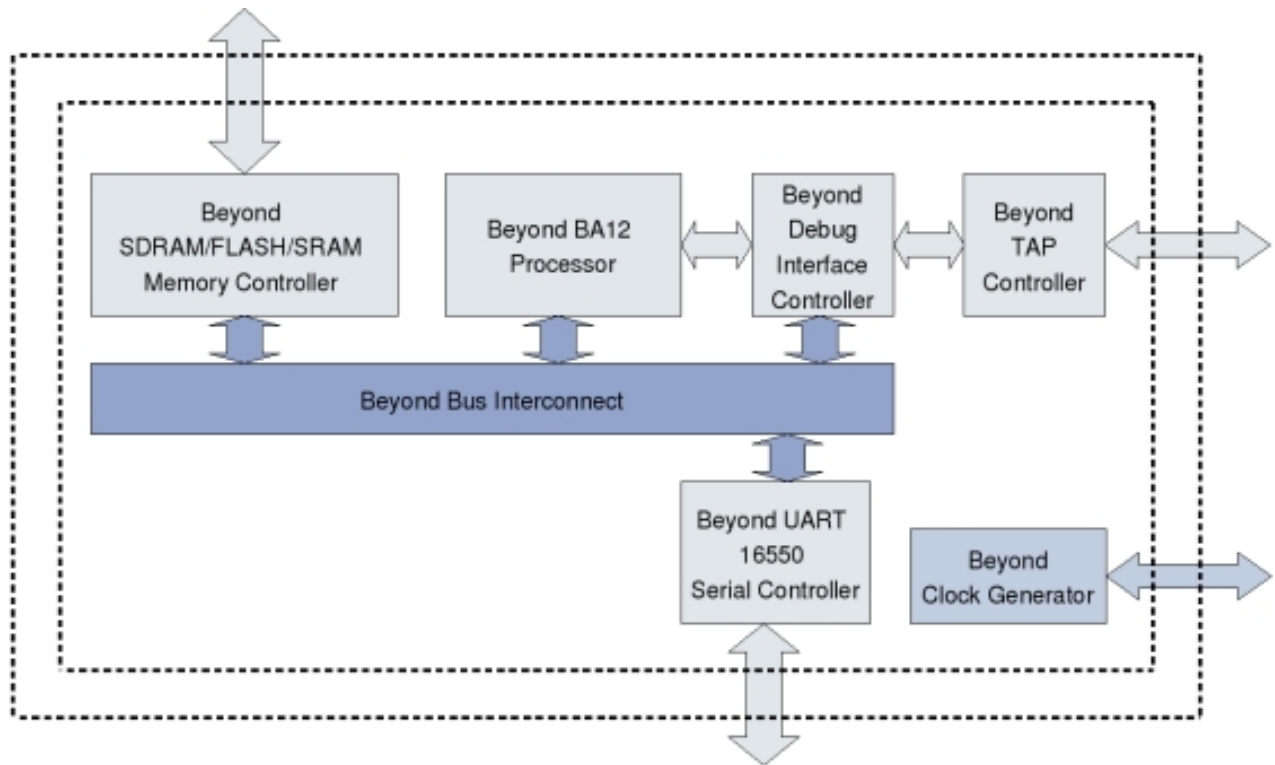
Third party software development tools will be available in the future.

Operating Systems

- Firmware

Target Applications

- Embedded
- Home entertainment consumer electronics
- Automotive
- Beyond BA12 testing
- Beyond BA12 software development
- IP development



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Utilization

The following table lists timing and area for a select list of implementation technologies.

Technology	Area	Speed	Power Consumption
XILINX Virtex2 (xc2v6000 ff1152 -5)	3000 Slices*	50 MHz	N/A
XILINX Virtex4 (xc4vlx60 ff668 -10)	3000 Slices*	70 MHz	N/A
XILINX Virtex4 (xc4vlx60 ff668 -12)	3330 Slices*	107 Mhz	N/A
ALTERA Stratix2 (ep2s60 f1020 c3es)	3760 ALUTs (2250 ALMs, 3000 LC comb., 2000 LC reg.)*	95 MHz	N/A
Structured ASIC 0.18um	75K Gates	160 MHz	N/A

* The design can be configured in numerous ways to be as optimal for a specific application. This changes the designs' area and speed.

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