BEYOND
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BEYOND BA25

High Performance 32-bit Application Processor

OVERVIEW

Beyond BA25 Advanced Application Processor (BA25), more powerful member of BA2x Family of 32-bit Processor IP Cores, is designed to fulfill the requirements of demanding embedded applications and is suitable as main processor for systems running general-purpose operating systems, such as Linux or Android.

Besides yielding smaller silicon footprint than most competing application processors, the BA25 operates at high clock frequencies and further utilizes benefits of highest code density in industry. Affordable silicon and license cost of this IP core enable our Customers development of notably differentiated and feature-rich products where not possible before.
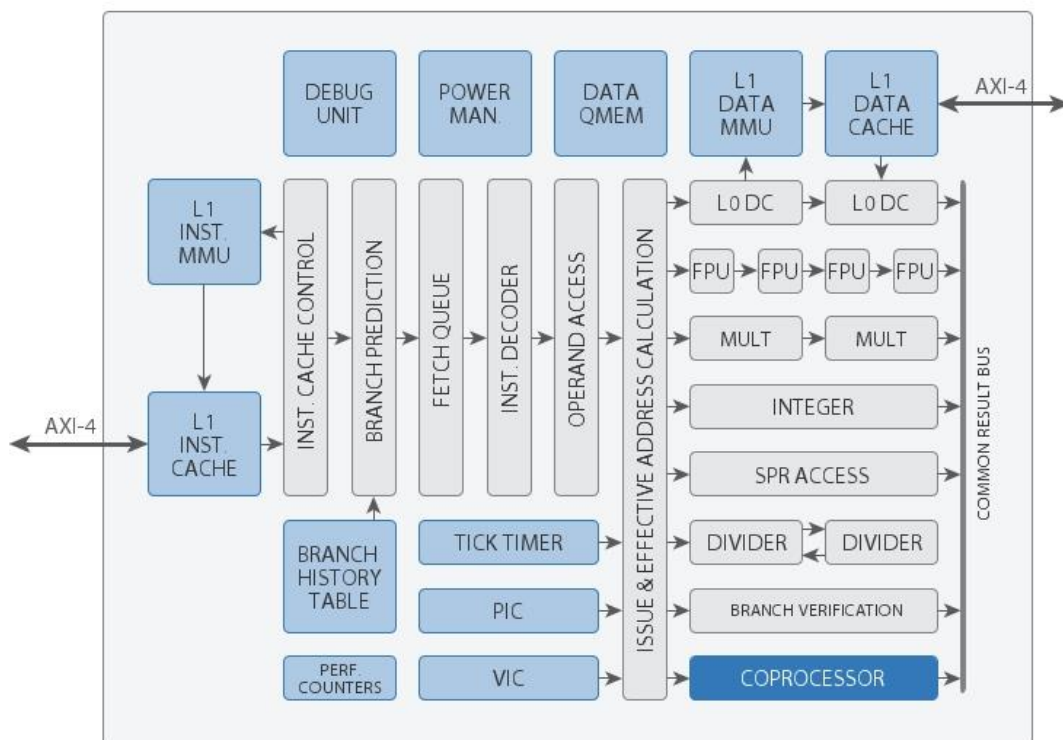
KEY BENEFITS

- 1.51 DMIPS/MHz, 800 MHz on 65 nm LP process;
- Independent functional units with out-of-order completion;
- Highest code density among Application Processors;
- Affordable silicon and license cost enables use of Application Processors and feature rich products where not possible before.

APPLICATIONS

- Set-top boxes and media players
- Image and video processing systems
- Wireless, battery-powered, or ultra-low-cost devices

BLOCK DIAGRAM

FEATURES

High Performance 32-bit CPU

- Seven-Stage Pipeline
- Out-of Order Completion
- Sophisticated Branch Prediction
- Optional Floating Point Unit
- 1.7 DMIPS/MHz
- 2.0 Coremarks/MHz
- 800+ MHz on TSMC 65nm LP

Efficient Power Management

- Dynamic clock gating and power shut-off of unused units
- Software- and hardware-controlled clock frequency
- Wake-up on tick timer or external interrupt

Fast & Flexible Memory Access

- Separate Instruction and Data Caches and MMU
- AXI4 data & instruction buses (32-, 64- or 128-bit) with 4 GBytes direct addressable space on each bus
- Tightly coupled Quick Memory (QMEM) interface for fast and deterministic access to code and/or data

Two-Level Cache and MMU

- L0 cache running at core frequency and L1 cache running at half the core frequency
- 1–16 Kbytes L0 caches, up to four-way set associative
- 32–512 Kbytes L1 caches, up to four-way set associative
- L0 MMU with up to 32 four-way associative entries
- L1 MMU with up to 2048 four-way associative entries

Optional Integrated Peripherals

- Vectored Interrupt Controller
- Microcontroller peripherals such as GPIO, UART, Real-Time Clock, Timers, I2C, and SPI
- Memory controllers, interconnect IP, and more

Easy Software Development

- Non-intrusive JTAG debug/trace for both CPU and system
- Complex chained watchpoint and breakpoint conditions
- BeyondStudio™ complete IDE for Windows or Linux under Eclipse
- Ported libraries and operating systems

THE BA2 INSTRUCTION SET

The BA2 instruction set provides extreme code density without compromises on performance, ease of use, or scalability. It features:

- A linear, 32-bit address space
- Variable length instructions: 16, 24, 32, or 48 bits
- Simple memory addressing modes
- A configurable number of 12 to 32 general purpose registers
- Efficient flow-control, arithmetic, and load/store instructions
- Floating point and DSP extensions

RELATED PRODUCTS

The BA2™ Processor Family includes a set of royalty-free, pre-configured products intended for different applications:

- BA22-DE Deeply Embedded Processor, for deeply embedded applications that use on-chip instruction and data memories.
- BA22-EM Embedded Processor, for deeply embedded applications that use off-chip instruction and data memories and that may need to run a real-time operating system (RTOS).
  BA22-AP Application Processor, for demanding embedded applications that may need to run an RTOS or OS.

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Founded in 2005, Beyond Semiconductor is addressing challenges of systemic complexity in today's electronic devices, empowering its customers to create new experiences for end users. Initially known for its processor expertise, Beyond quickly gained acceptance among top semiconductor companies and evolved into global company leveraging processing, software and system-wide view competence to provide its customers with effectively designed IP and ASICs.
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